

**PATENT APPLICATION**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Shinji HIRANO

Application No.: 10/762,474

Filed: January 23, 2004

For: SEMICONDUCTOR INTEGRATED CIRCUIT INCLUDING FUSE DEVICE AND  
METHOD FOR MANUFACTURING THE SAME



Group Art Unit: 2826

Examiner: F. ERDEM

Docket No.: 118267

**REQUEST FOR RECONSIDERATION**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

In reply to the April 24, 2006 Office Action, the period for reply being extended by the attached Petition for Extension of Time, reconsideration of the rejection and objections is respectfully requested in light of the following remarks.

Claims 1-20 are pending in this application. Claims 1-6 and 14-16 are withdrawn from consideration.

Claims 7, 9, 11 and 17-19 are rejected under 35 U.S.C. §103(a) over U.S. Patent No. 5,252,844 to Takagi in view of U.S. Patent No. 6,335,228 to Fuller et al. (Fuller). The rejection is respectfully traversed.

Claim 7 recites, *inter alia*, "an electrode that contacts the semiconductor region at a periphery of a bottom of the contact hole."

According to Fuller, a fuse oxide layer 910 is grown over the implanted region 810 in the anti-fuse area 20 (Fig. 9). A second layer of doped polysilicon 912 is then deposited (Fig. 9). However, as shown in Fig. 10, the fuse oxide layer 910 covers the entire bottom surface

of the anti-fuse contact hole and does not permit the doped polysilicon 912 (electrode) to contact the implanted region (the semiconductor region) 810 at a periphery of the bottom of the contact hole. Thus, Takagi in view of Fuller cannot reasonably be considered to teach or suggest an electrode that contacts the semiconductor region at a periphery of a bottom of the contact hole, as recited in independent claim 7.

Therefore, it is respectfully submitted that claim 7 is patentable over Takagi in view of Fuller. Claims 9, 11 and 17-19 are patentable over Takagi in view of Fuller at least in view of the patentability of claim 7 from which they depend, as well as for the additional features they recite. Accordingly, withdrawal of the rejection under 35 U.S.C. §103(a) is respectfully requested.

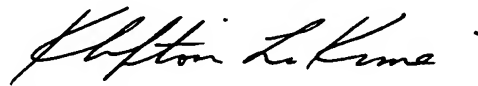
Upon allowance of claims 7, 9, 11 and 17-19, rejoinder and allowance of claims 1-6 and 14-16 are respectfully requested. Applicant respectfully submits that the withdrawn method claims are closely related to the pending apparatus claims such that, having searched for the features recited in the apparatus claims, no further search should be necessary, or at least any further search would be limited and not create an undue burden.

In particular, claim 1 recites a method for manufacturing a semiconductor integrated circuit, and claim 7 recites a semiconductor integrated circuit having every element provided or formed by the method of claim 1, as follows. Claim 7 recites "a semiconductor substrate having a fuse device" and claim 1 recites "providing a semiconductor substrate having a fuse device." Claim 7 recites "an interlayer insulating film" and claim 1 recites "forming an interlayer insulating film." Claim 7 recites "the interlayer insulating film having ... a contact hole ... a central portion of the contact hole having a columnar insulator region" and claim 1 recites "forming a contact hole ... such that a columnar insulator region ... is formed in the central portion of the contact hole." Finally, claim 7 recites "an electrode" and claim 1 recites "forming an electrode."

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1-20 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,



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Date: October 23, 2006

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